REMARKS

Claims 1-18 stand rejected.

Claims 1, 4, 5, 6, 15, and 18 are currently amended.

Claims 2, 3, 14, 16, and 17 are cancelled herewith.

Claims 1, 4-13, 15 and 18 are now pending.

Support for the amendments to claims 1, 6, and 15 may be found in the specification, for example in paragraphs [0038], [0039], [0046], and [0047].

Rejection of Claims under 35 U.S.C. § 101

Appreciation is expressed for the entry of the After Final Amendment dated April 6, 2007, and the subsequent withdrawal of the 35 U.S.C. § 101 rejection of claims 15-18.

Rejection of Claims under 35 U.S.C. § 103

Claims 1-3, 5-8, 10, and 12-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, U.S. Patent No. 5,659,801 ("Kopsaftis"), in view of Torrey et al., U.S. Patent Appl. No. 2003/0084240 ("Torrey"). Applicants respectfully traverse this rejection.

As amended, independent claim 1, and generally independent claim 6 recite, inter alia, "said first LUN processes I/O commands, and said second LUN processes microcode update commands,...said first device obtaining a LUN address from each of said one or more commands, in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device...**storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored***

***microcode in said first device**, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated*"(emphasis added).

In re claims 1 and 6, the Office Action states Kopsaftis teaches a method including "assigning a first LUN to a first device…said first device receiving one or more commands…said first device obtaining a LUN address from each of said one or more commands…" (*Office Action, paragraph 10).*

The Office Action recognizes that Kopsaftis fails to explicitly teach assigning a second LUN to a memory and states that Torrey teaches assigning a first LUN to a first device and assigning a second LUN to a memory (see Office Action paragraph 10).

The Office Action relies upon the combination of Kopsaftis and Torrey to teach that in response to said LUN address obtained from each of said one or more commands being equal to said LUN, updating said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands.

The cited portion of Kopsaftis discloses when "the initiator command is detected, no transfer of data is performed...[i]nstead the disk drive enters a state ready to receive new microcode….the resident processor 106, now under the control of the resident microcode in non-volatile memory 108 clears a buffer in the resident RAM 110 of sufficient size to hold the new microcode when an initiator command is detected" (*Kopsaftis column 8, line 63 through column 9, line 2*).

The cited portions of Kopsaftis fails to teach that in response to said LUN address obtained from each of said one or more commands *being equal to said second*

*LUN, said first device**...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in said first device**, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated*" (emphasis added).

The cited portions of Torrey teach the use of "logical unit numbering to address different portions of the library" (Torrey, paragraph [0015]) and that if a "request is directed to only a portion or specific elements of the library, the library controller uses the SCSI LUN assigned to the storage elements, media and I/O elements involved to carry out the request..." (Torrey, paragraph [0020]).

The cited portions of Torrey fails to teach that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device**...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in said first device**, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated.*

The cited portions of Kopsaftis and Torrey, either alone or in combination, do not disclose that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device**...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in*

***said first device**, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated.*

Accordingly, Applicants submit that all of the claim limitations of independent claims 1 and 6 have not been shown by Kopsaftis and Torrey, alone or in combination as required by § 706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claims 1 and 6. Accordingly, Applicants respectfully submit that claims 1 and 6 are allowable for at least this reason over Kopsaftis and Torrey, either alone or in combination.

Claim 5 depends from independent claim 1 and are allowable for at least this reason. Claims 7-8, 10, and 12-13 depend from independent claim 6, and are allowable for at least this reason.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Shirasawa et al., U.S. Patent Appl. No. 2002/0166027 ("Shirasawa").

In re claim 4, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 1. Accordingly, as claim 4 depends from claim 1, Applicant respectfully submit that all of the claim limitations of claim 4 have not been shown by Kopsaftis and Torrey in view of Shirasawa, alone or in combination. Accordingly, Applicants respectfully submit that claim 4 is allowable for at least this reason over Kopsaftis, Torrey and Shirasawa, either alone or in combination.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Pellegrino et al., U.S. Patent Appl. No. 2004/0225775 ("Pellegrino").

In re claim 9, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 6. Accordingly, as claim 9 depends from claim 6, Applicant respectfully submit that all of the claim limitations of claim 9 have not been shown by Kopsaftis and Torrey in view of Pellegrino, alone or in combination. Accordingly, Applicants respectfully submit that claim 9 is allowable for at least this reason over Kopsaftis, Torrey and Pellegrino, either alone or in combination.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Abbott et al., U.S. Patent No. 6,205,093 ("Abbott").

In re claim 11, Applicants submit above that the combination of Kopsaftis and Torrey fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 6. Accordingly, as claim 11 depends from claim 6, Applicant respectfully submit that all of the claim limitations of claim 11 have not been shown by Kopsaftis and Torrey in view of Abbott, alone or in combination. Accordingly, Applicants respectfully submit that claim 11 is allowable for at least this reason over Kopsaftis, Torrey and Abbott, either alone or in combination.

Claims 15-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis and Torrey in further view of Burton et al., U.S. Patent No. 6,393,535 ("Burton").

As amended, independent claim 15 recites, inter alia, "said first LUN processes I/O commands, and said second LUN processes microcode update commands,...said first device obtaining a LUN address from each of said one or more commands, in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device*...***storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in said first device,*** *and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated*"(emphasis added).

In re claim 15, the Office Action states Kopsaftis teaches a method including "assigning a first LUN to a first device...said first device receiving one or more commands...said first device obtaining a LUN address from each of said one or more commands..." (*Office Action, paragraph 10).*

The Office Action recognizes that Kopsaftis fails to explicitly teach assigning a second LUN to a memory and states that Torrey teaches assigning a first LUN to a first device and assigning a second LUN to a memory (see Office Action paragraph 10).

The Office Action relies upon the combination of Kopsaftis and Torrey to teach that in response to said LUN address obtained from each of said one or more commands being equal to said LUN, updating said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands.

The cited portion of Kopsaftis discloses when "the initiator command is detected, no transfer of data is performed...[i]nstead the disk drive enters a state ready to receive new microcode....the resident processor 106, now under the control of the resident microcode in non-volatile memory 108 clears a buffer in the resident RAM 110 of sufficient size to hold the new microcode when an initiator command is detected" (*Kopsaftis column 8, line 63 through column 9, line 2*).

The cited portions of Kopsaftis fails to teach that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device****...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in said first device****, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated*" (emphasis added).

The cited portions of Torrey teach the use of "logical unit numbering to address different portions of the library" (Torrey, paragraph [0015]) and that if a "request is directed to only a portion or specific elements of the library, the library controller uses the SCSI LUN assigned to the storage elements, media and I/O elements involved to carry out the request..." (Torrey, paragraph [0020]).

The cited portions of Torrey fails to teach that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device****...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in***

response, updating said stored microcode in said first device*, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated.*

The Office Action states Burton "teaches an article of manufacture comprising a data storage medium tangibly embodying a program of machine-readable instruction executed by a processing apparatus to perform method steps" (*Office Action paragraph 27).*

The cited portion of Burton does not disclose that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device****...storing said microcode in said memory using said LUN address assigned to said second LUN by processing each of said one or more commands, and in response, updating said stored microcode in said first device****, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated.*

The cited portions of Kopsaftis, Torrey, and Burton either alone or in combination, do not disclose, that in response to said LUN address obtained from each of said one or more commands *being equal to said second LUN, said first device****...storing said microcode in said memory using said LUN address assigned to said second LUN***

by processing each of said one or more commands, and in response, updating said stored microcode in said first device, and receiving at least one of a verification command and an operational test command to verify that said microcode has been updated.

Accordingly, Applicants submit that all of the claim limitations of independent claim 15 have not been shown by Kopsaftis, Torrey, and Burton, alone or in combination as required by § 706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claim 15. Accordingly, Applicants respectfully submit that claim 15 is allowable for at least this reason over Kopsaftis, Torrey, and Burton either alone or in combination.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, and Burton, in further view of Shirasawa.

In re claim 18, Applicants submit above that the combination of Kopsaftis, Torrey and Burton fail to teach or suggest all of Applicants claim limitations in, at least, independent claim 15. Accordingly, as claim 18 depends from claim 15, Applicant respectfully submit that all of the claim limitations of claim 18 have not been shown by Kopsaftis, Torrey, Burton and Shirasawa, alone or in combination as required by §706.02 (j) of the MPEP. It follows then that a *prima facie* case of obviousness has not been met with respect to claim 18. Accordingly, Applicants respectfully submit that claim 18 is allowable for at least this reason over Kopsaftis, Torrey, Burton and Shirasawa, either alone or in combination.

CONCLUSION

Applicants have amended claims 1, 6, and 15 and cancelled claims 2-3, 14, 16-17 from further consideration in this application. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

In view of the remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at the numbers provided below.

I hereby certify that this correspondence is being submitted via Electronic Filing System to: Commissioner for Patents, Mail Stop, Alexandria, VA, 22313-1450, herewith:

Halka Gordon — 07.16.07
Halka Gordon — Date of Signature

Respectfully submitted,

Jennifer M. Anda
Reg. No. 58,436
Phone: (520) 799-2485
Facsimile: (520) 799-5551